[Document Name] Specification

[Title of the Invention] OVERLAY MARK, METHOD OF MEASURING OVERLAY ACCURACY, METHOD OF MAKING ALIGNMENT AND SEMICONDUCTOR DEVICE THEREWITH

[Claims]

[Claim 1] An overlay mark having a mark pattern formed by engraving a groove or an indent in a prescribed position on a layer where a circuit pattern is formed, and a grooved pattern that surrounds said mark pattern so as to protect said mark pattern from being deformed by thermal expansion or contraction of said layer.

[Claim 2] An overlay mark used for measuring the overlay accuracy in forming a second circuit pattern over a first circuit pattern; which has:

a first lower-layer pattern formed by engraving a groove or an indent in a prescribed position on a first layer where the first circuit pattern is formed, and an upper-layer pattern formed in a prescribed position on a second layer where the second circuit pattern is to be formed; and, in addition,

a second lower-layer pattern that is formed by engraving, on the first layer, a frame-shaped groove to surround the first lower-layer pattern, and is not used for measuring the overlay accuracy.

[Claim 3] The overlay mark according to Claim 2, wherein the first lower-layer pattern is utilized as an alignment mark at the time of alignment to superimpose a mask onto